Instruction manual

DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER
Program Card Set
909/919-1417

025-1417

REV B FEB 81

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FOREWORD

Before attempting to use the 909-1417 Program Card Set in a Data I/O Model 1, 2, 7, 9 or Programmer Satellite, read the following.

Models 1 & 2: Pin NN of the Programmer MEU must be jumpered to ground before this cardset can be used. Program and Read operations can be done only in the AUTO mode.

Models 7 & 9: This card set cannot be used in a Model 7 & 9 with Revision "A" software. A software upgrade can be obtained through your nearest Data I/O Service Center.

Programmer Satellite: This card set cannot be used with the Programmer Satellite.

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
INTEL				
1024x8 MOS	8741/8748	VOH TS	40 PIN	1448
2048x8 MOS	8755	VOL TS	40 PIN	1447-1
2048x8 MOS	8755A	VOL TS	40 PIN	1447-2

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences and shapes of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909-part number. See Figure 1-1 b).

1.2 PROGRAMMING ALGORITHM

The card set begins the program operation with a backwards device test. If the device is mis-socketed, the programmer stops. Otherwise, it proceeds to the program and verify cycles.

The card set activates the program mode and applies an address to the device. It then tests for a bit to program and, if necessary, applies the program data along with a program pulse. Each address is programmed completely before the card set moves on to the next address.

1.3 CALIBRATOR PROGRAM ADAPTER

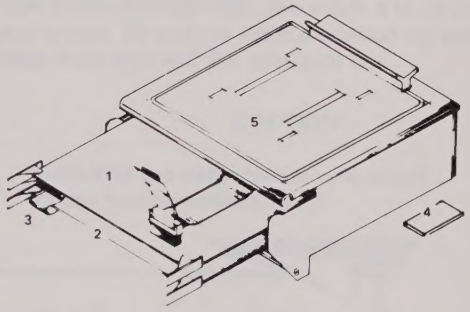
The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

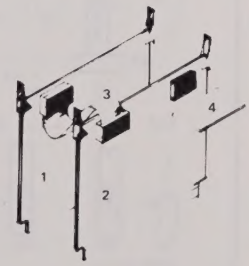
1.4 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1-9 Programmers

1. DIGITAL CARD	701-1418
2. ANALOG CARD	701-1417
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1417
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

Table 2-1. Customer-Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP1	Reject	A	Reject after one pulse

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 and 2 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

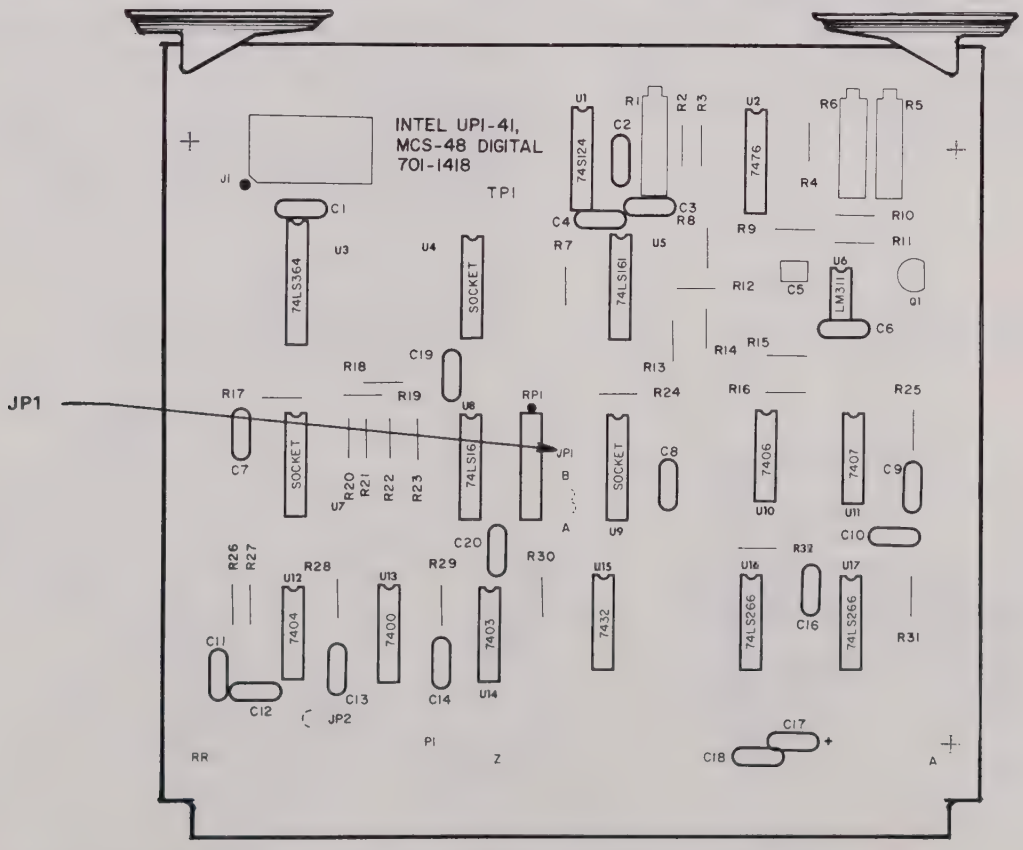


Figure 2-1. Digital Card Jumper Locations

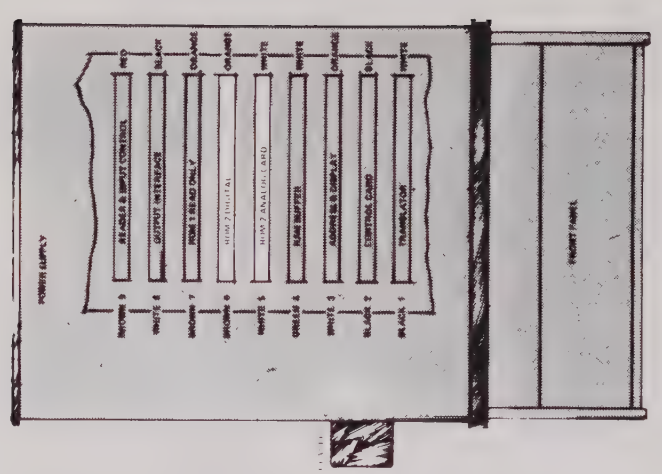


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down — the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

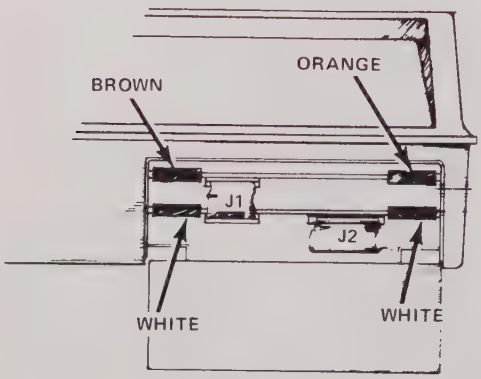


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

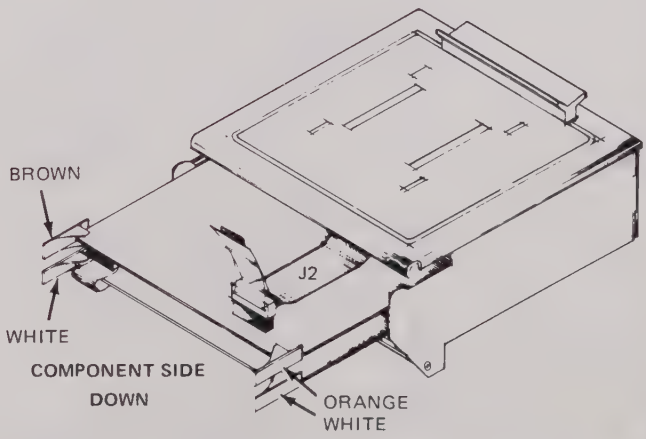


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4
CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

a. Data I/O Universal Calibrator, P/N 910-1071

b. Calibration Extender:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1521

c. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.

d. A potentiometer adjustment tool

e. Dual-trace oscilloscope — Tektronix 465 or equivalent

f. A jumper wire approximately 12 inches in length

g. Data I/O interconnection cables:

Models 1-5	P/N 709-1613
Model 9	P/N 709-2608, 709-1613
System 19	P/N 709-2612, 709-1613

h. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1-5

Refer to Figure 4-1.

a. Make sure the programmer power is OFF.

b. Remove the cover from the programmer and remove the Program Card Set from the card cage.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

d. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

RESET
ROM2 — ROM2
MANUAL
PROGRAM
START

Figure 4-1. Set-up of Models 1-5 for DC Calibration.

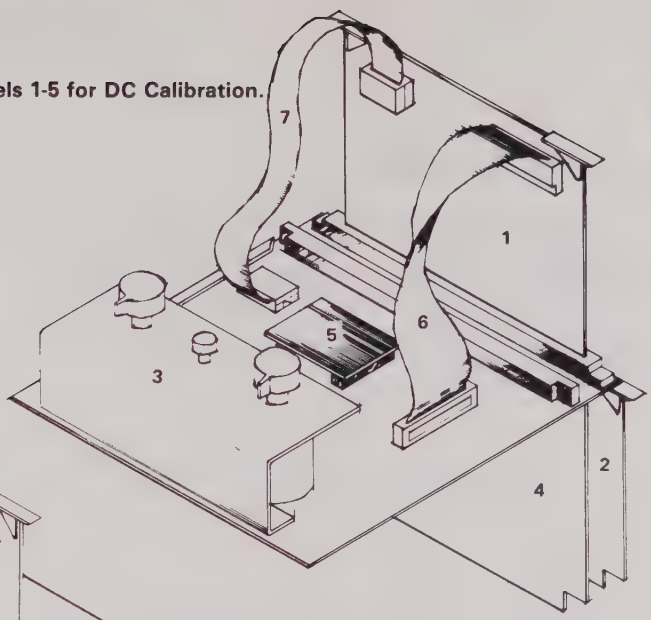
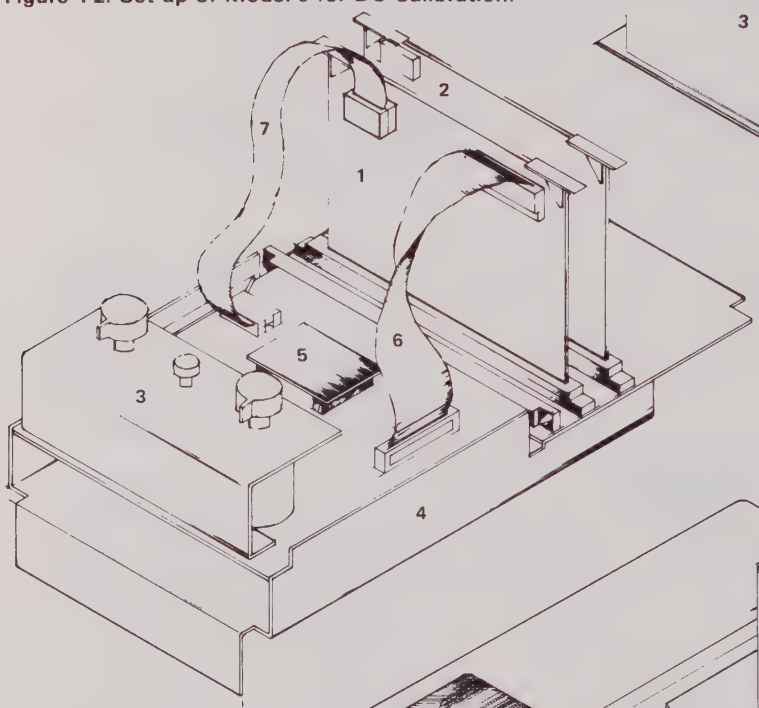
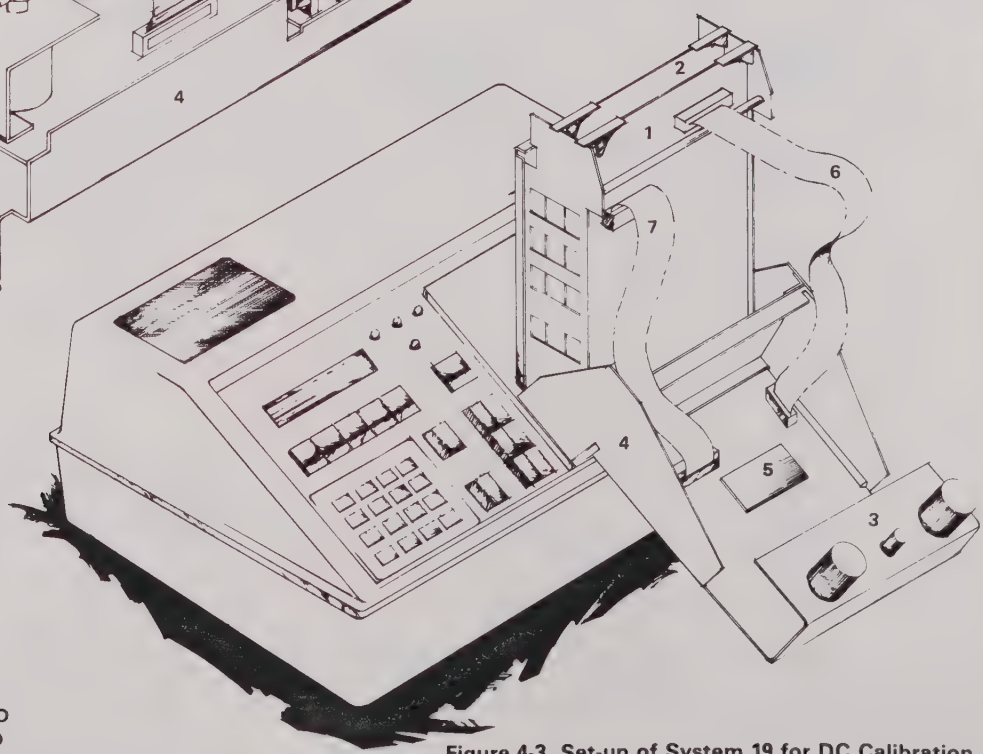


Figure 4-2. Set-up of Model 9 for DC Calibration.





1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATION EXTENDER
5. CALIBRATOR PROGRAM ADAPTER
6. 26-CONDUCTOR CABLE
7. 16-CONDUCTOR CABLE

Figure 4-3. Set-up of System 19 for DC Calibration.

4.2.2 MODEL 9

Refer to Figure 4-2.

a. Make sure the programmer power is OFF.

b. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

c. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the analog card.

d. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's digital card position (brown/orange). Be sure that the edge of the Extender Card is securely seated. Install the Digital and Analog cards into the 1074 calibration extender according to Figure 4-2.

e. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

f. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

g. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

h. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

KEYBOARD
EXECUTE
NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

a. Make sure the programmer power is OFF.

b. Remove the Programming Pak from the programmer.

c. Insert the Calibration Extender, P/N 910-1521, in the same way as the Programming Pak, being sure to seat it properly in the programmer's mating connector.

d. With the handle of the Programming Pak down, connect the 64-pin connectors of the Programming Pak and Calibration Extender. Be sure the connectors mate securely.

e. Slide the Universal Calibrator securely into the card slots at the front of the Calibration Extender.

f. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe with the connector dot.

g. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe with the connector dot.

h. Plug the Calibrator Program Adapter into the Program Adapter slot on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 919-XXXX part number of the Programming Pak.

i. Connect the DVM ground lead to GND test point on the Universal Calibrator.

j. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

SELECT
C1 (calibrate ON)
START

k. Press:

KEYBD
ENTER

The TEST light comes ON and remains ON throughout calibration.

NOTE
To exit calibration, press:
SELECT
C0 (calibrate OFF)
START
(Test light goes OFF.)

l. Press START.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

- The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

- The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

- The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

- The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the Calibration Chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

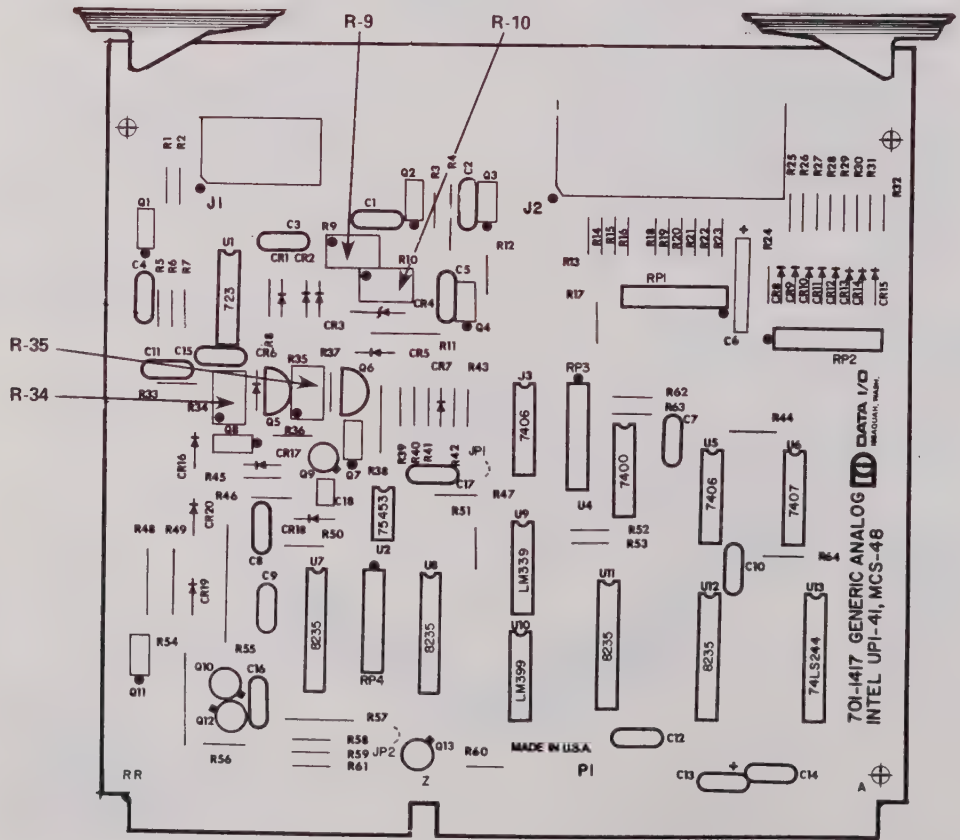


Figure 4-4. Analog Card Adjustment Locations

Calibration Chart

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CALIBRATION CHART 017-1417 | PROGRAM CARD 909-1417
FIXTURE 702-1071 | MANUFACTURER Intel
PROGRAM ADAPTER 910-1417 | PROM 8741, 8748, 8755, 8755A

DATE	REV	REVISION RECORD	DR	CK
5-78	A	RELEASE	GJ	GJ
8-78	B	CN #2407	RT	KJ
4-79	—	CN # 2565	FS	
3-13-80	B	ECN #3504	KJB	
3-10-81	B	ECN #4008	EF	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX	COMMENTS
FF	FA	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5	Adjustments located on power supply board. See programmer manual.
FF	FA	POWER +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8	
FF	FA	SUPPLIES +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15	
FF	FA	-9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8	
FF	FA	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		30.0		33.0	
FF	FE	VCC PROGRAM, VERIFY (1)	2-1	001	01	001	5	1	TP3	R34	4.8	5.0	5.2	*Adjustment Step.*
FF	FE	VCC CURRENT LIMIT, RESET	2-2	001	01	001	6	1						Confirm programmer in STOP.
FF	FE	VEA HIGH (2)	3-1	001	01	001	2	23	TP3	R35	22.5	23.0	23.5	*Adjustment Step.* Set Programmer in START.
FF	FE	VDD VERIFY (3)	4-1	001	01	001	4	21	TP3	R9	4.8	5.0	5.2	*Adjustment Step.*
FF	FA	VDD PROGRAM	4-2	002	02	002	4	21	TP3	R10	24.1	24.3	24.5	*Adjustment Step.*
FF	FA	PROG/VDD HIGH (4)	5-1	003	03	003	4	6	TP3		24.0		24.5	
FF	FA	VDD, PROG/VDD LIMIT, RESET	5-2	003	03	003	5	21						Confirm programmer in STOP. Set Programmer in START.
FF	FB	PROG/VDD FLOAT	5-3	004	04	004	10	6	TP3		5.0		5.2	
FF	F9	PROG/VDD LOW	5-4	005	05	005	10	6	TP3		0.0		0.2	
FF	7A	VDD KILL	6-1	006	06	006	2	21	TP3		0.0		1.0	
FF	7A	VCC KILL	6-2	006	06	006	2	1	TP3		0.0		0.5	
FF	7A	VEA LOW	7-1	006	06	006	2	23	TP3		0.0		1.0	
9F	F7	TØ HIGH (5)	8-1	007	07	007	7	9	TP3		5.0		5.2	
9F	F7	RD LOW (6)	8-2	007	07	007	7	8	TP3		0.0		0.2	
9F	F7	PROG/CE LOW (7)	8-3	007	07	007	7	7	TP3		0.0		0.2	
9F	F7	RESET/ALE LOW (8)	8-4	007	07	007	7	10	TP3		0.0		0.2	
9F	F7	XTAL 1 HIGH	8-5	007	07	007	4	12	TP3		2.0		2.45	
9F	F7	CONFIGURE 1 LOW	8-6	007	07	007			J1-14				0.2	Test point located on analog card.
9F	F7	CONFIGURE 2 LOW	8-7	007	07	007	10	22	TP3		0.0		0.2	
F7	EB	TØ LOW	8-8	008	08	010	7	9	TP3		0.0		0.2	
F7	EB	$\overline{RD}$ HIGH	8-9	008	08	010	7	8	TP3		5.0		5.2	
F7	EB	PROG/CE HIGH	8-10	008	08	010	7	7	TP3		5.0		5.2	
F7	EB	RESET/ALE HIGH	8-11	008	08	010	7	10	TP3		5.0		5.2	
F7	EB	XTAL 1 LOW (9)	8-12	008	08	010	7	12	TP3		0.0		0.4	

COMMENTS
- Use paragraphs 4.3.1-4.3.5 for key sequences for COMMENTS below.
- Switch S1 must be depressed for accurate readings.
- CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
F7	EB	CONFIGURE 1 HIGH	8-13	008	08	010			J1-14		5.0		5.2
F7	EB	CONFIGURE 2 HIGH	8-14	008	08	010	10	22	TP3		5.0		5.2
F7	EB	PULL-UP TEST	8-15	008	08	010	2	5	TP3		2.35		2.70
F7	EB	COMPARATOR REF. LOW	9-1	008	08	010	2	5	R51		1.9		2.2
FF	7F	COMPARATOR REF. HIGH	9-2	009	09	011	2	5	R51		2.35		2.70
FD	FF	BIT 8 COMPARATOR	10-1	011	0B	013	3	13					
FD	FF	BIT 7 COMPARATOR	10-2	011	0B	013	3	14					
FD	FF	BIT 6 COMPARATOR	10-3	011	0B	013	3	15					
FD	FF	BIT 5 COMPARATOR	10-4	011	0B	013	3	16					
FD	FF	BIT 4 COMPARATOR	10-5	011	0B	013	3	17					
FD	FF	BIT 3 COMPARATOR	10-6	011	0B	013	3	18					
FD	FF	BIT 2 COMPARATOR	10-7	011	0B	013	3	19					
FD	FF	BIT 1 COMPARATOR	10-8	011	0B	013	3	20					
FD	BF	VOL DATA BIT 8 VIL	11-1	012	0C	014	7	13	TP3		0.0		0.2
FD	BF	VOL DATA BIT 7 VIH	11-2	012	0C	014	7	14	TP3		5.0		5.2
FD	BF	VOL DATA BIT 6 VIL	11-3	012	0C	014	7	15	TP3		0.0		0.2
FD	BF	VOL DATA BIT 5 VIH	11-4	012	0C	014	7	16	TP3		5.0		5.2
FD	BF	VOL DATA BIT 4 VIL	11-5	012	0C	014	7	17	TP3		0.0		0.2
FD	BF	VOL DATA BIT 3 VIH	11-6	012	0C	014	7	18	TP3		5.0		5.2
FD	BF	VOL DATA BIT 2 VIL	11-7	012	0C	014	7	19	TP3		0.0		0.2
FD	BF	VOL DATA BIT 1 VIH (10)	11-8	012	0C	014	7	20	TP3		5.0		5.2
FF	BF	VOH DATA BIT 8 VIH	11-9	013	0D	015	7	13	TP3		5.0		5.2
FF	BF	VOH DATA BIT 7 VIL	11-10	013	0D	015	7	14	TP3		0.0		0.2
FF	BF	VOH DATA BIT 6 VIH	11-11	013	0D	015	7	15	TP3		5.0		5.2
FF	BF	VOH DATA BIT 5 VIL	11-12	013	0D	015	7	16	TP3		0.0		0.2
FF	BF	VOH DATA BIT 4 VIH	11-13	013	0D	015	7	17	TP3		5.0		5.2
FF	BF	VOH DATA BIT 3 VIL	11-14	013	0D	015	7	18	TP3		0.0		0.2
FF	BF	VOH DATA BIT 2 VIH	11-15	013	0D	015	7	19	TP3		5.0		5.2
FF	BF	VOH DATA BIT 1 VIL	11-16	013	0D	015	7	20	TP3		0.0		0.2
FF	BF	VOH DATA BIT 8 VIL	11-17	013	0D	015	7	13	TP3		0.0		0.2
FF	BF	VOH DATA BIT 7 VIH	11-18	013	0D	015	7	14	TP3		5.0		5.2
FF	BF	VOH DATA BIT 6 VIL	11-19	013	0D	015	7	15	TP3		0.0		0.2

CALIBRATION CHART 017-1417

PAGE 2 OF 4

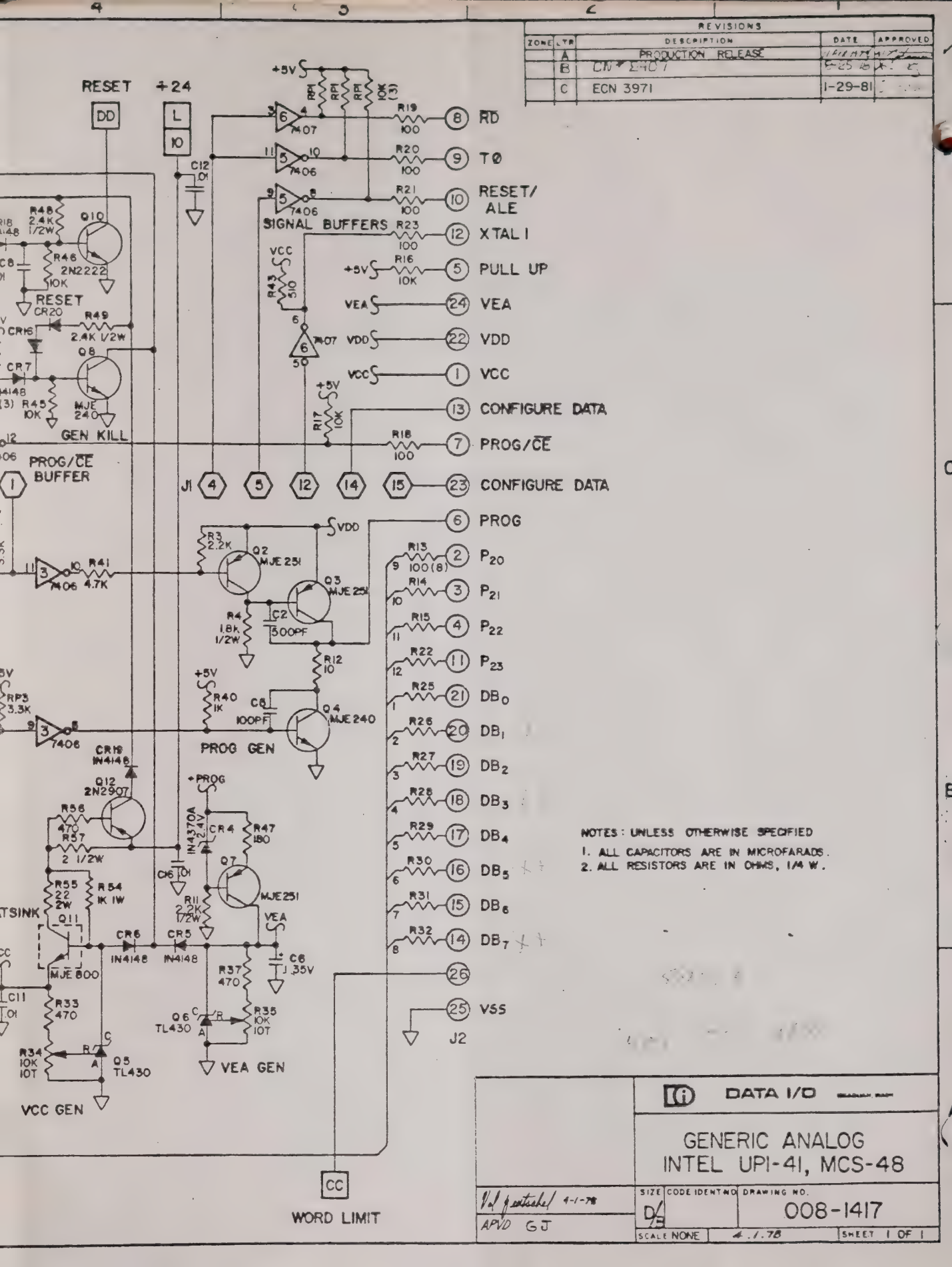
	MODEL 5	9	19	
Test point located on analog card.				
Test point: Bottom of R51 on analog card.				
Confirm	Bit 8 ON	7F	7F	DO Bus
Confirm	Bit 7 ON	BF	BF	DO Bus
Confirm	Bit 6 ON	dF	dF	DO Bus
Confirm	Bit 5 ON	EF	EF	DO Bus
Confirm	Bit 4 ON	F7	F7	DO Bus
Confirm	Bit 3 ON	FB	FB	DO Bus
Confirm	Bit 2 ON	FD	FD	DO Bus
Confirm	Bit 1 ON	FE	FE	DO Bus
LOAD	Bits 2,4,6,8,ON	AA	55	DI Bus
Confirm	Bits 2,4,6,8,ON	55	55	DO Bus
LOAD	N/A	NA	AA	DI Bus
Confirm	Bits 2,4,6,8,ON	55	AA	DO Bus
LOAD	Bits 1,3,5,7,ON	55	55	DI Bus
Confirm	Bits 1,3,5,7,ON	AA	55	DO Bus

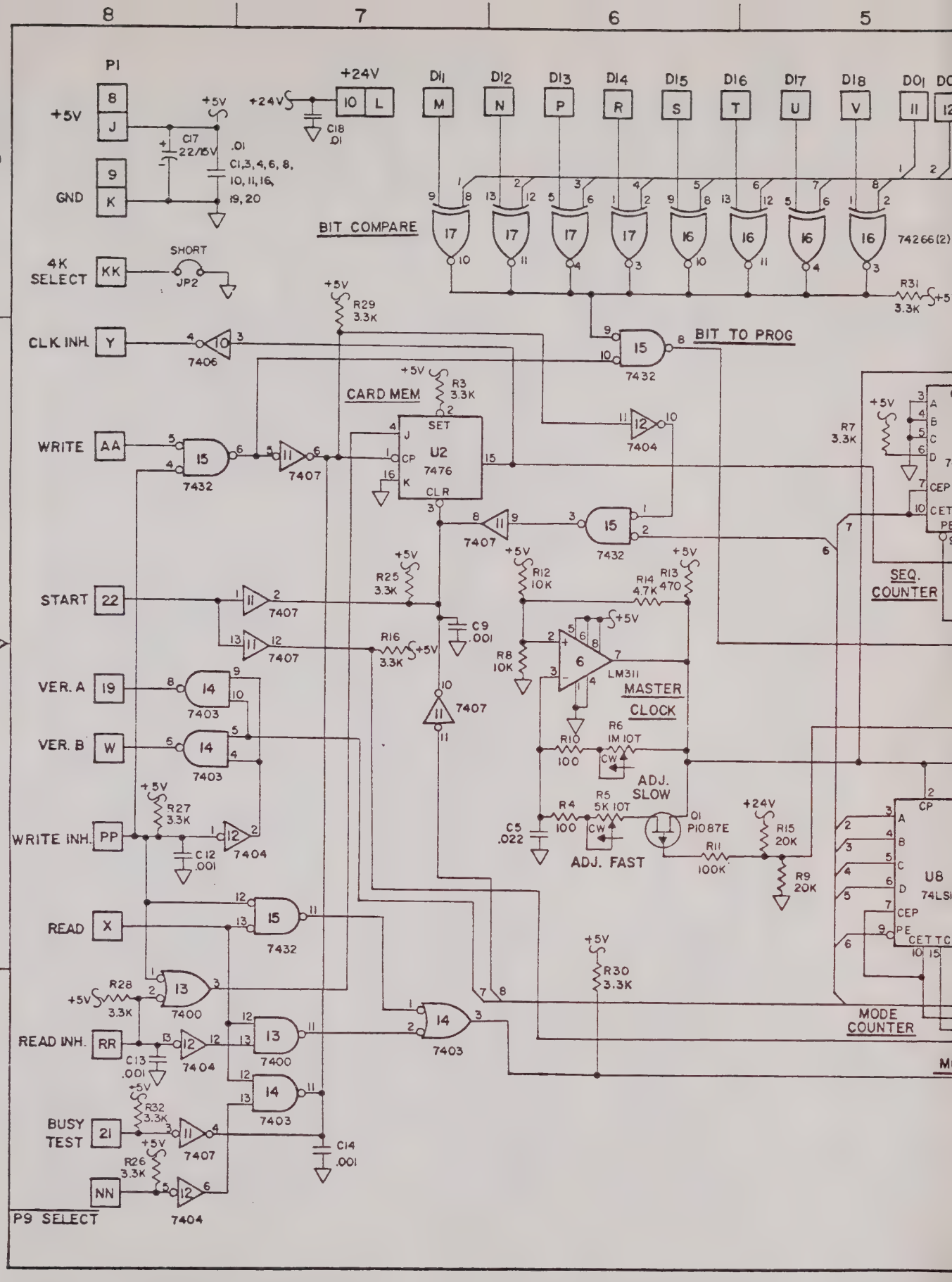
CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U 2	U 1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
FF	BF	VOH DATA BIT 5 VIH	11-20	013	0D	015	7	16	TP3		5.0		5.2
FF	BF	VOH DATA BIT 4 VIL	11-21	013	0D	015	7	17	TP3		0.0		0.2
FF	BF	VOH DATA BIT 3 VIH	11-22	013	0D	015	7	18	TP3		5.0		5.2
FF	BF	VOH DATA BIT 2 VIL	11-23	013	0D	015	7	19	TP3		0.0		0.2
FF	BF	VOH DATA BIT 1 VIH	11-24	013	0D	015	7	20	TP3		5.0		5.2
FD	BF	VOL DATA BIT 8 VIH	11-25	014	0E	016	7	13	TP3		5.0		5.2
FD	BF	VOL DATA BIT 7 VIL	11-26	014	0E	016	7	14	TP3		0.0		0.2
FD	BF	VOL DATA BIT 6 VIH	11-27	014	0E	016	7	15	TP3		5.0		5.2
FD	BF	VOL DATA BIT 5 VIL	11-28	014	0E	016	7	16	TP3		0.0		0.2
FD	BF	VOL DATA BIT 4 VIH	11-29	014	0E	016	7	17	TP3		5.0		5.2
FD	BF	VOL DATA BIT 3 VIL	11-30	014	0E	016	7	18	TP3		0.0		0.2
FD	BF	VOL DATA BIT 2 VIH	11-31	014	0E	016	7	19	TP3		5.0		5.2
FD	BF	VOL DATA BIT 1 VIL	11-32	014	0E	016	7	20	TP3		0.0		0.2
7F	BF	DATA DISABLE	12-1	015	0F	017							
FF	7F	BACKWARDS DEVICE TEST	13-1	017	011	021	3	20			(SEE NOTE 1)		
FF	DF	ADDRESS TEST VIH, A0	14-1	1365	555	2525	7	20	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A1	14-2	1365	555	2525	7	19	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A2	14-3	1365	555	2525	7	18	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A3	14-4	1365	555	2525	7	17	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A4	14-5	1365	555	2525	7	16	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A5	14-6	1365	555	2525	7	15	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A6	14-7	1365	555	2525	7	14	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A7	14-8	1365	555	2525	7	13	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A8 (11)	14-9	1365	555	2525	7	2	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A9	14-10	1365	555	2525	7	3	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A10	14-11	1365	555	2525	7	4	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A11	14-12	1365	555	2525	7	11	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIL, A0	14-13	2730	AAA	5252	7	20	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A1	14-14	2730	AAA	5252	7	19	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A2	14-15	2730	AAA	5252	7	18	TP3		0.0		0.2
FF	DF	ADDRESS TEST VIH, A3	14-16	2730	AAA	5252	7	17	TP3		5.0		5.2
FF	DF	ADDRESS TEST VIL, A4	14-17	2730	AAA	5252	7	16	TP3		0.0		0.2

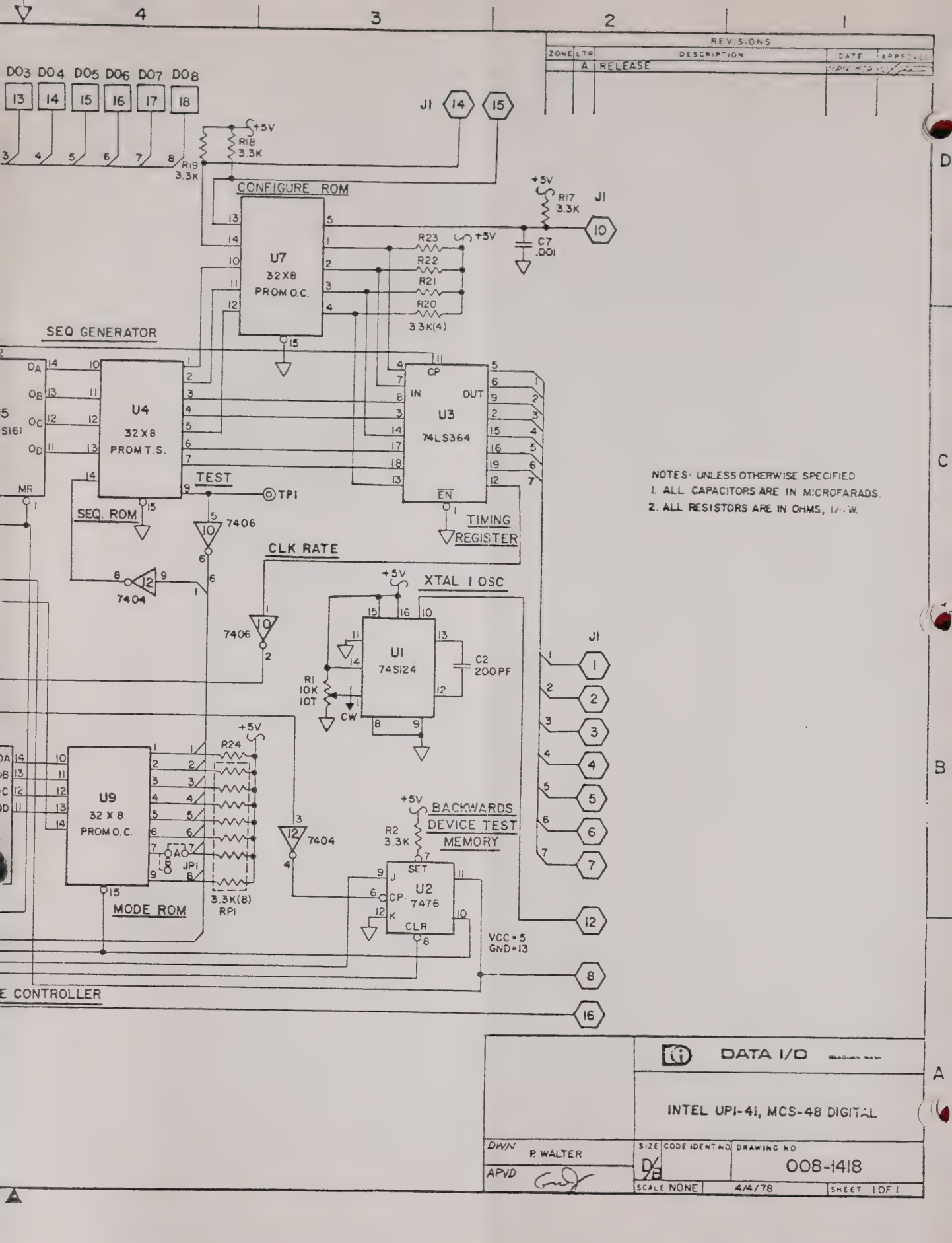
CALIBRATION CHART 017-1417

CONT.		MODEL 5	9	19	
	LOAD	Bits 1,3,5,7,ON	55	55	DI Bus
	Confirm	Bits 1,3,5,7,ON	AA	55	DO Bus
	LOAD	N/A	N/A	AA	DI Bus
	Confirm	Bits 1,3,5,7,ON	AA	AA	DO Bus
	LOAD	All Bits ON	FF	FF	DI Bus
	Confirm	All Bits OFF	00	00	DO Bus

NOTE:
1. Set programmer in STOP. Press S1 on calibrator and hold to simulate backwards device while attempting to set programmer in START. Programmer must remain in STOP.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A PRODUCTION RELEASE
B CN# 2407
C ECN 3971 1-29-81
RESET
+24
DD
L
10
+5V
RP1 RP2 RP3 RP4 10K
7407
7406
R19 100
R20 100
R21 100
R23 100
R16 10K
R43 510
R17 10K
R18 100
C12 01
SIGNAL BUFFERS
8 RD
9 T0
10 RESET/ ALE
12 XTAL I
5 PULL UP
24 VEA
22 VDD
1 VCC
13 CONFIGURE DATA
7 PROG/CE
23 CONFIGURE DATA
6 PROG
2 P20
3 P21
4 P22
11 P23
21 DB0
20 DB1
19 DB2
18 DB3
17 DB4
16 DB5
15 DB6
14 DB7
26
25 VSS
J2
J1 4 5 12 14 15
R48 2.4K 1/2W
Q10
R46 2N2222 10K
RESET
CR20
R49 2.4K 1/2W
CR16
Q8
CR7
R45 10K
MJE 240
GEN KILL
PROG/CE BUFFER
R41 4.7K
RP3 3.3K
R3 2.2K
Q2 MJE 251
Q3 MJE 251
R4 1.8K 1/2W
C2 500PF
R12 10
R40 1K
C8 100PF
Q4 MJE 240
PROG GEN
R13 100(8)
R14
R15
R22
R25
R26
R27
R28
R29
R30
R31
R32
CR18 IN4148
Q12 2N2907
R56 470
R57 2 1/2W
+PROG
IN4370A 2.4V
CR4
R47 180
Q7 MJE251
C6 01
R11 2.2K 1/2W
VEA
R55 22 2W
R54 1K 1W
Q11 MJE 800
CR6 IN4148
CR5 IN4148
C6 1.35V
R37 470
R33 470
R34 10K 10T
Q5 TL430
Q6 TL430
R35 10K 10T
VEA GEN
VCC GEN
CC
WORD LIMIT
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS, 1/4 W.
DATA I/O
GENERIC ANALOG
INTEL UPI-41, MCS-48
Val Gottschalk 4-1-78
APVD GJ
SIZE D/E
CODE IDENT NO
DRAWING NO. 008-1417
SCALE NONE
4.1.78
SHEET 1 OF 1


8
7
6
5
D
C
B
A
P1
+5V
GND
J
K
C17 22/15V
.01
C1,3,4,6,8,10,11,16,19,20
+24V
L
C18 .01
D11
D12
D13
D14
D15
D16
D17
D18
DO1
M
N
P
R
S
T
U
V
11
BIT COMPARE
17
16
74266(2)
R31 3.3K
4K SELECT
KK
SHORT
JP2
R29 3.3K
CLK INH.
Y
7406
BIT TO PROG
7432
CARD MEM
R3 3.3K
WRITE
AA
U2
7476
SET
CP
CLR
7407
7404
R7 3.3K
SEQ. COUNTER
START
22
R25 3.3K
R12 10K
R14 4.7K
R13 470
C9 .001
R16 3.3K
R8 10K
LM311
MASTER CLOCK
VER. A
19
7403
VER. B
W
R6 1M 10T
R10 100
CW
ADJ. SLOW
R27 3.3K
WRITE INH.
PP
C12 .001
R4 100
R5 5K 10T
C5 .022
ADJ. FAST
Q1 P1087E
R11 100K
R15 20K
R9 20K
U8
74LS
CEP
CET
PE
TC
READ
X
R28 3.3K
READ INH.
RR
C13 .001
R30 3.3K
MODE COUNTER
BUSY TEST
21
R32 3.3K
R26 3.3K
NN
C14 .001
P9 SELECT


4
3
2
1
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A RELEASE
D03 D04 D05 D06 D07 D08
13 14 15 16 17 18
J1 14 15
+5V
R18 3.3K
R19 3.3K
CONFIGURE ROM
U7 32X8 PROM O.C.
+5V
R17 3.3K
J1
10
C7 .001
R23 R22 R21 R20 3.3K(4)
+5V
SEQ GENERATOR
U4 32X8 PROM T.S.
U3 74LS364
CP
IN
OUT
EN
TEST
TP1
SEQ. ROM
7406
TIMING REGISTER
CLK RATE
7404
7406
+5V
XTAL I OSC
U1 74S124
R1 10K 10T
CW
C2 200PF
J1
1
2
3
4
5
6
7
+5V
R24
U9 32 X 8 PROM O.C.
JP1
3.3K(8) RP1
MODE ROM
7404
+5V
BACKWARDS DEVICE TEST MEMORY
R2 3.3K
U2 7476
SET
CP
CLR
12
VCC=5
GND=13
8
16
E CONTROLLER
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN MICROFARADS.
2. ALL RESISTORS ARE IN OHMS, 1/4 W.
DATA I/O
INTEL UPI-41, MCS-48 DIGITAL
DWN P. WALTER
APVD
SIZE D/B
CODE IDENT NO
DRAWING NO 008-1418
SCALE NONE
4/4/78
SHEET 1 OF 1

- The TEST POINT column gives test point locations for the DVM probe. Most test points are located on the Universal Calibrator; some points are located on the program card. For instance, if a test point is designated as U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

- The LIMITS column is divided into three portions: MIN (minimum), NOM (nominal), and MAX (maximum). The values given are in volts and indicate the range into which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the programmer (or Program Card Set) passes a particular test. If a reading falls outside of the given limits, or if it cannot be adjusted to fall within the limits (in adjustment steps), the card is nonfunctional and should not be used for programming.

- The COMMENTS column on the right side of the chart provides information for certain calibration steps including call-outs of programmer operations required in some steps. The programmer provides signals to the card set on the Address bus, the Data Input bus, the START/STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set the following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4.3.1 — 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer to paragraphs 4.3.1 — 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions of software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5:	Observe the START and STOP indicators.
Model 9:	Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.
System 19:	Observe the START light. If the START light is on, the programmer is in START.

4.3.2 SET THE STATE OF THE START/STOP LINE

Models 1, 2, 3 and 5:	Press the START/STOP key.
Model 9:	a. Press KEYBOARD to stop.
	b. Press EXECUTE to start.
System 19:	a. To set the programmer in START, press KEYBD, ENTER and START.
	b. To set programmer in STOP, press KEYBD.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5:	Press the FWD key or the REV key.
Model 9:	See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.
Revision "A" Software:	Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:
	a. Ground J1-16 on the analog card.
	b. Press LOAD.
	c. Press EXECUTE.
	d. Press KEYBOARD.
	e. Key in data — Ø hex — at address ØØ1.
	f. Press VERIFY.
	g. Press EXECUTE. The programmer will mis-verify

at the address containing data and will STOP in FWD.

h. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD. Press ENTER and then REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the Calibration Chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) Key in the Model 9 hex data called out in the "Comments" column.

Revision "A" Software: Halt the programmer in the automatic program mode with data on the DI bus.

a. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.

b. Press the KEYBOARD key, and key in hex data called out on the Calibration Chart.

c. Press the PROGRAM key.

d. Ground J1-16 on the analog card.

e. Press EXECUTE and wait for the programmer to abort.

f. Press STOP, KEYBOARD and EXECUTE.

g. Disconnect J1-16 from ground.

h. SET the address specified on the Calibration Chart in order to make the measurement.

Revision "B" or later Software: With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in Model 9 hex data called out on the Calibration Chart.

System 19:

a. Press KEYBD, key in the address and press ENTER.

b. Key the System 19 hex data into RAM at the specified address.

c. Press ENTER and then REVIEW.

4.3.5 CONFIRM DATA ON THE DO BUS

Models 1, 2, 3 and 5: Compare the bit callout on the Calibration Chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF. Ignore the hex data on the chart.

Model 9: With the EXECUTE light ON, press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the Calibration Chart.

System 19: With KEYBD selected, press the DEVICE DATA key. Hold it down while reading the hex data. The programmer must be in START.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the Timing Diagram, have the same reference on the Calibration Chart. Waveforms are selected using Universal Calibrator switches S2 and S3 as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

a. Make sure that the programmer power is OFF.

b. Remove the digital card from the card slot.

c. Check the Timing Diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

d. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.

e. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.

f. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the Timing Diagram. Connect an input probe to TP3 on the calibrator.

g. Reinstall the digital card in the slot from which it was removed.

h. Check the NOTES column on the Timing Diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1—5, press:	RESET RAM-RAM PROGRAM MANUAL START
Model 9:	Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the Timing Diagram specifies the correct polarity. Press: KEYBOARD.
System 19 press:	KEYBD Ø ENTER

3. Key in data for bit 1 at several addresses:

Models 1—5:	Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.
Model 9:	Enter hex data "Ø1" at several addresses.
System 19:	Enter hex data "Ø1" at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the Timing Diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets. Return to address ØØØ.

4. Select the PROGRAM mode:

Models 1 — 5, press:	RESET PROGRAM AUTO RAM-ROM2

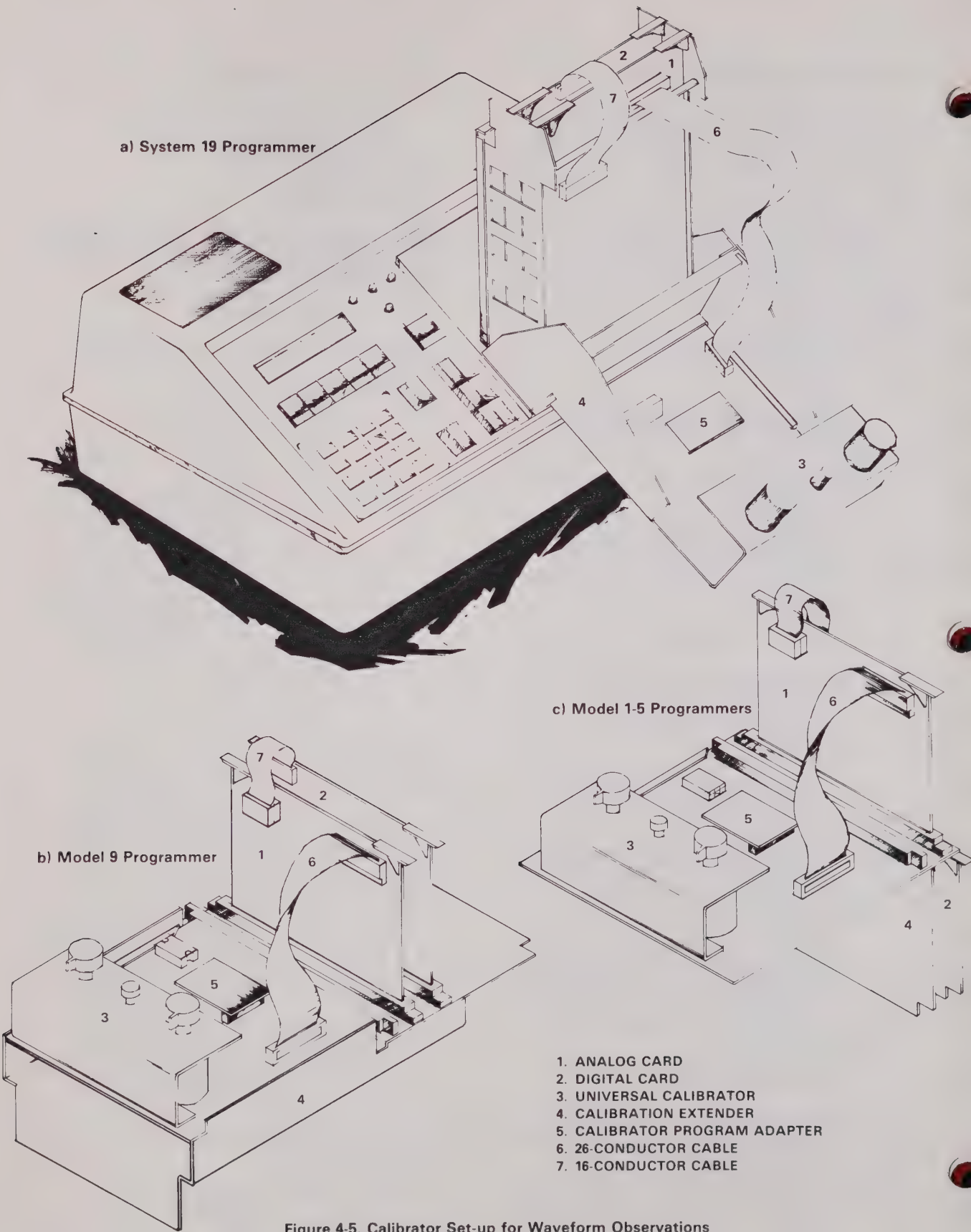
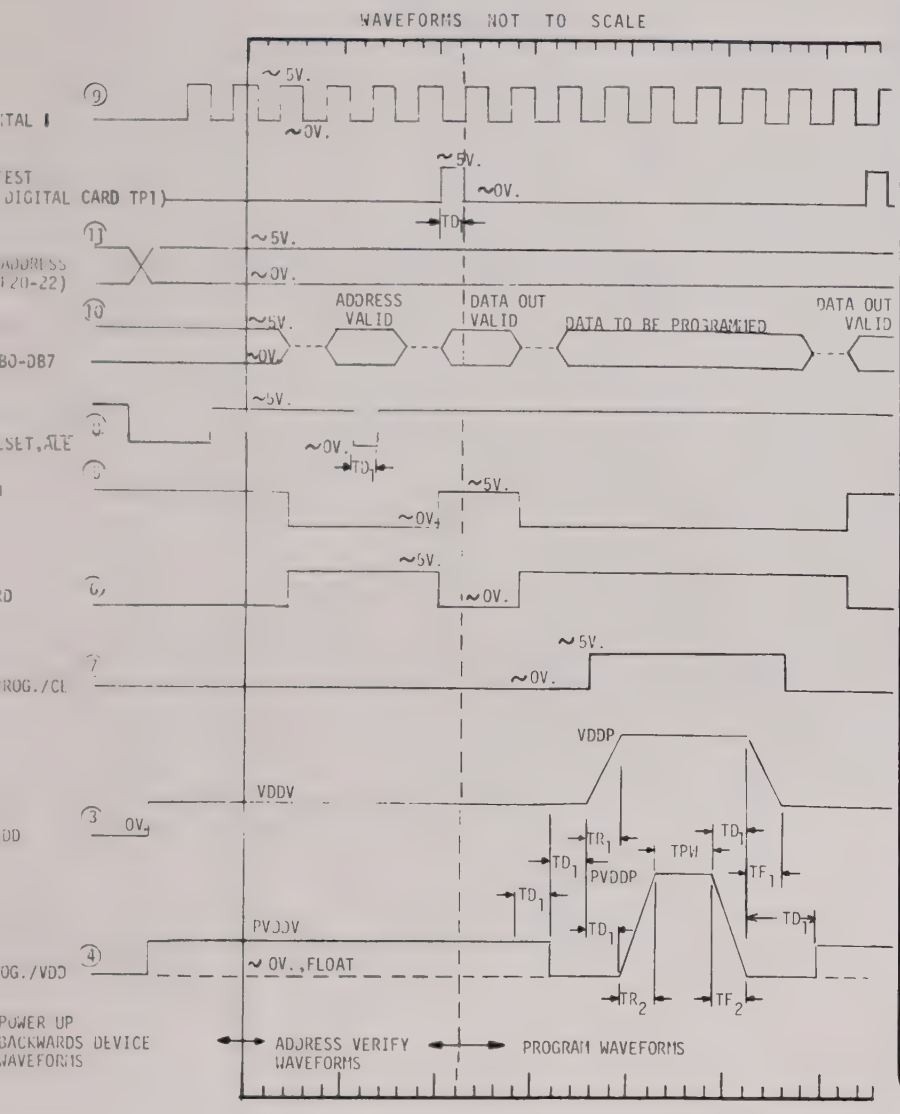


Figure 4-5. Calibrator Set-up for Waveform Observations

DATE	SYM	REVISION RECORD	DR.	CK
4-25-78	A	RELEASE	PW	
8-28-78	B	CN# 2407		
2-2-79	-	ECN #2594	FS	



NOTES

DIGITAL CARD JUMPERS

JP1 = 1 PULSE REJECT = POS. A
JP1 = NO REJECT = POS. B
JP2 = SHORT

WAVEFORM VARIABLES

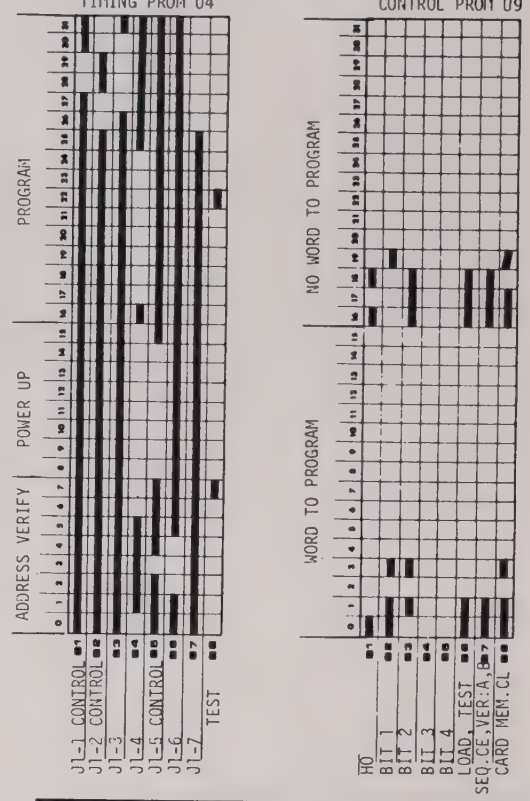
CLK RATE (FAST), ADJUST R5 FOR TD
CLK RATE (SLOW), ADJUST R6 FOR TPW
TD_1 = 200 ± 20 us
TPW = 55 ± 5 ms
TR_2=TF_2 = .5 TO 2 us
XTAL I PERIOD = 750 ± 50 ns Adjust R1
VCC = 5.00 ± 0.20 V.
VDDV = 5.00 ± 0.20 V.
VDDP = 24.3 ± 0.2 V.
PVDDV = VDDV(8755A) = 0 V. (8755)
= FLOAT (8741/48)
PVDDP = VDDP
VEAH = 23.0 ± 0.5 V.
VEAL = -1 V.
TR_1 = TF_1 = 10-100 us

○ These waveforms correspond to call-outs on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Performance Check section of manual for detailed steps.

For calibration, the card set polarity defaults to VOH.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)



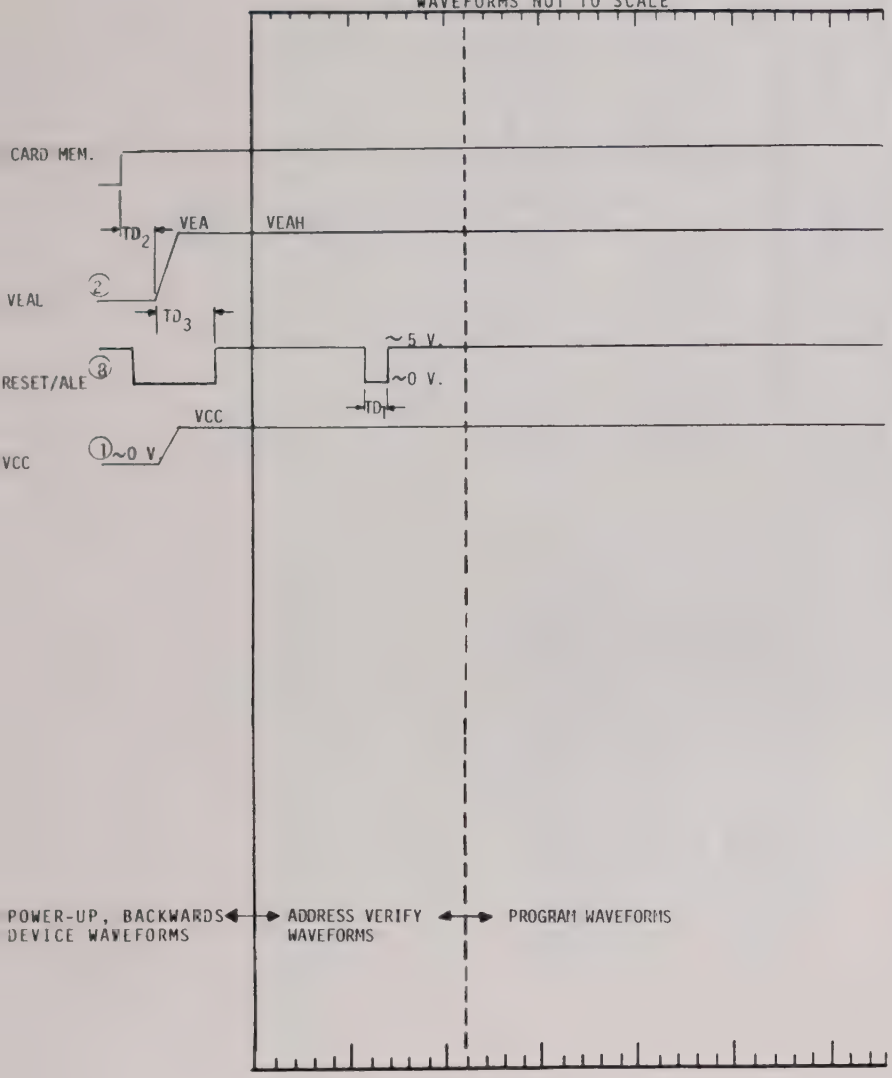
DATA I/O ISSAQUAH, WASH.

TIMING DIAGRAM	DRAWN BY P. WALTER
	APPROVED BY
TITLE: INTEL UPI-41, MCS-48	
DATE: 4-25-78	DRAWING NUMBER: 007-1417

DATE/BY	REVISION RECORD	ECN
	See Sheet 1 of 2	

(WAVEFORMS CONTINUED)

WAVEFORMS NOT TO SCALE



NOTES

WAVEFORM VARIABLES

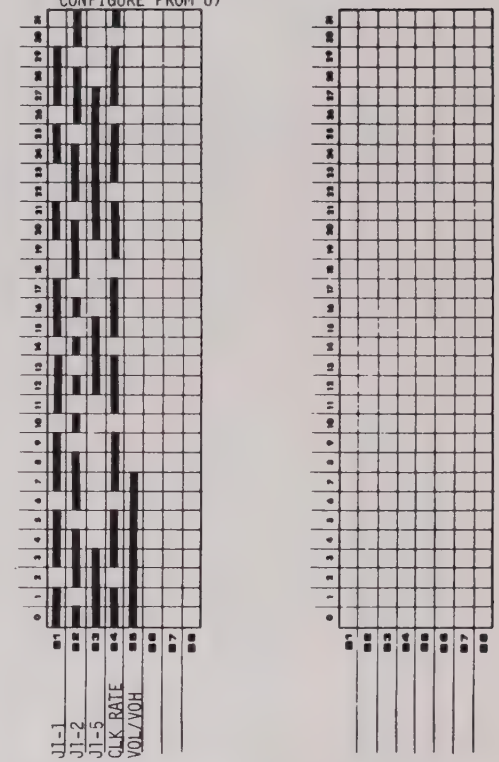
VCC = 5 ± .2 V.
VEAH = 23.0 ± .5 V.
VEAL = ~1 V.
TD_1 = 200 us ± 20 us
TD_2 = ~3 ms
TD_3 = ~1.5 ms

For calibration, the card set polarity defaults to VOH.

TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

CONFIGURE PROM U7



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TIMING DIAGRAM	DRAWN BY P. WALTER
TITLE INTEL UPI-41, MCS-48	
DATE 4-25-78	DRAWING NUMBER 007-1417

Sheet 2 of 2

Model 9, press: PROGRAM

System 19, press: PROG

5. Initiate waveforms:

Models 1 — 5, press: START

Model 9, press: EXECUTE

System 19, press: START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the Timing Diagram and Calibration Chart by the circled digits (1 , 2 , 3 , ...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the Calibration Chart is of no importance during waveform observation.

CAUTION

When S1 is depressed, high currents are induced within the programmer; do not hold S1 depressed for extended periods.

6. Stop programming:

Models 1 — 5 and 9, press: STOP

System 19, press KEYBD

4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

CAUTION

The reject jumper must be reinstalled. Otherwise, the device's programming specifications will be violated, and the programmer and/or cardset may be damaged by a prolonged attempt to program a defective device.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Ground J1-16.
6. With the Universal Calibrator switches set to observe PROG/VDD, connect the scope probe to TP3 on the Universal Calibrator and trigger on TP3.
7. Repeat the key sequence in the waveform Test Procedure, 4.4.2 steps 1-5. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort functions of the digital card is operative. The System 19 will display Error 22.

NOTE

The digital card has one or more potentiometers for calibrating various timing functions of the card set. In normal usage, the card set will rarely need to have these functions re-calibrated.

However, in the event that the card set waveforms do not conform to the specifications of the Timing Diagram contact your nearest Data I/O Service Representative for calibration information.

SECTION 5
CIRCUIT DESCRIPTION

5.1 INTRODUCTION

Data I/O Program Card Sets consist of a Digital Card, an Analog Card, and interconnecting cables. Both cards interface with the Programmer and with each other. The analog card interfaces with the PROM being programmed. Figure 5-1 gives a generalized block diagram of the relations between the cards, the Programmer, and the PROM being programmed or read.

5.1.1 DIGITAL CARD

The digital card receives data from the Programmer on the DI Bus, and from the PROM on the DO Bus. These data are compared at each bit of each PROM word both before and after programming. At each bit, the digital card continues to command PROM program pulses from the analog card until either ABORT or REJECT is signalled or until the bit is programmed.

5.1.2 ANALOG CARD

The analog card receives bit addresses, word addresses, timing, and mode commands. Analog card output consists of PROM manufacturers' specified programming voltages and currents. When specified by the manufacturer, each programmed PROM bit is tested for loading and/or leakage. Following the program cycle, PROMs are read by the analog card to verify that programmed data matches truth table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain functional operation of the analog card and the digital card. Also included are discussions of signal flow, timing and reject conditions. Detailed circuit schematics are found at the rear of this manual — refer to these for pin-out and interconnection information.

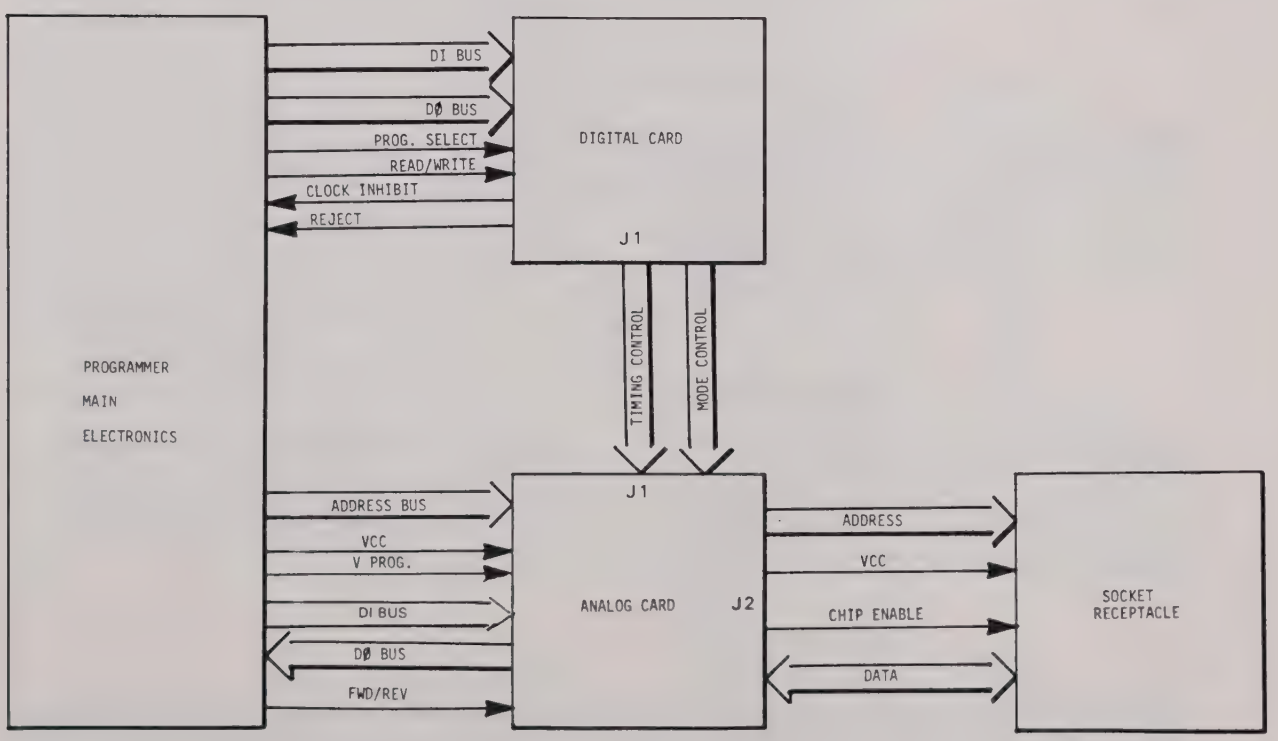


Figure 5-1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

The digital card block diagram is shown in Figure 4-2. The digital card receives control signals from the programmer bus as shown in the diagram on the left side, and outputs control signals to the analog card as shown on the right.

5.2.1 SELECT AND CONTROL GATING

The select and control gates monitor the programmer status lines in order to enable operation of the digital card. Outputs supply data to the Card Memory, control the VFY A and VFY B lines for selecting 4/8 bit operation and announcing an abort condition.

The analog card receives a signal from these gates that enables the analog card Data Bus Drivers to output to the programmer DO bus.

5.2.2 CARD MEMORY

This memory serves as the interface ("handshake") control of the card set to the programmer main electronics. When the card set is selected for operation, the Card Memory sets upon either a Write, Read or Busy Test Pulse. This causes the digital card to begin operation. Before the Card Memory sets, the Sequence Counter and Backwards Device Test Memory are reset.

5.2.3 MASTER CLOCK

The two-speed clock is free-running with its rate controlled by the clock rate line of the Sequence Generator. The slower clock rate is enabled during the program pulse time (TPW) and the faster clock rate during Verify and Test times. Parallel timing is used so that all counters and memories (except the Program Memory) receive the same clock pulse.

5.2.4 BACKWARDS DEVICE TEST MEMORY

To prevent damage to a mis-socketed device, a Backwards Device Test is performed before power is applied to the device. The Backwards Device Test Memory, when not set, enables the Backwards Device Test to be performed. On Start, the Mode Controller advances until a Mode Counter carry is output. This carry sets the Backwards Device Test Memory. Before this memory sets, and while the controller is running, a backwards device will pull reset. Once this memory is set, backwards device testing is disabled and power is applied to the device.

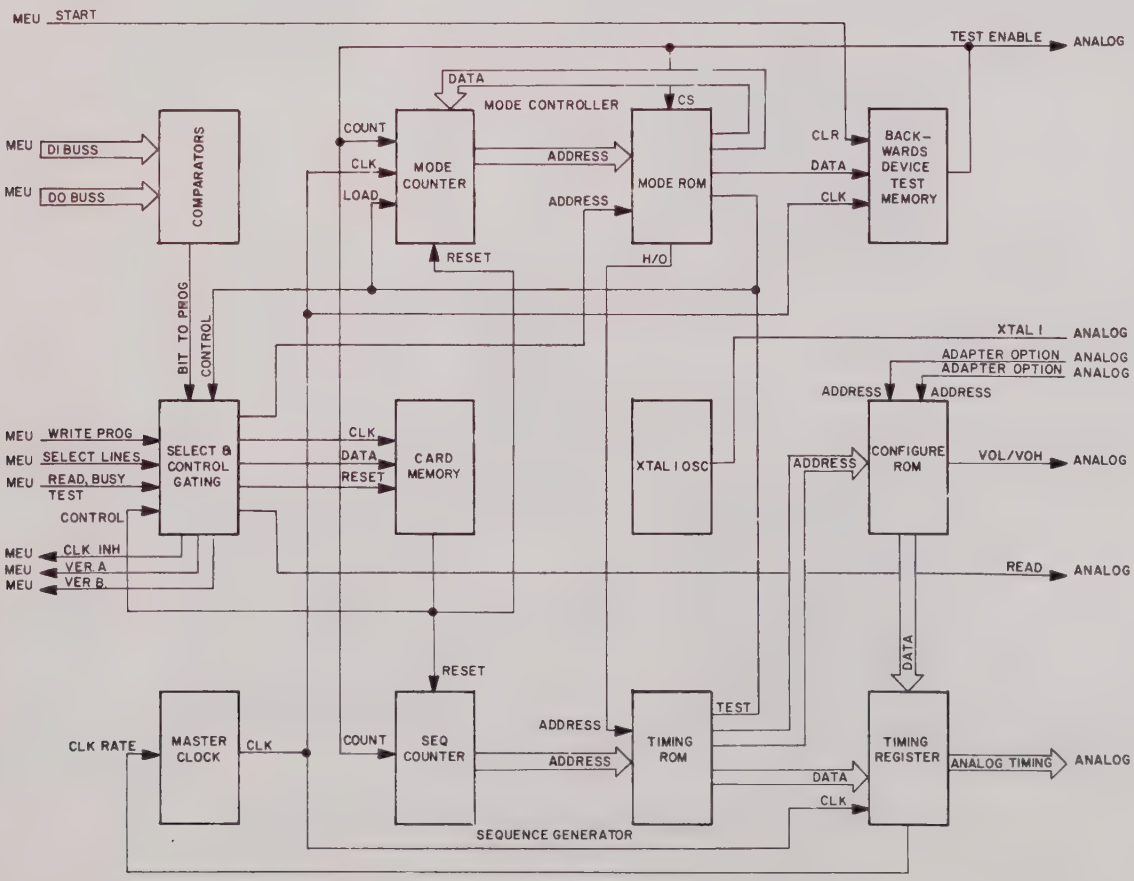


Figure 5-2. Block Diagram, 1418 Digital Card

5.2.5 MODE CONTROLLER

The Mode Controller consists of a 4-bit counter and a 32x8 ROM. When the Card Memory sets, the Sequence Counter advances to Test, enabling the controller. The controller provides digital-card control during Verify and Program operations. The controller sends the high-order address input to the Sequence ROM. This input is held low during Verify and Read operations and high during Program.

5.2.6 COMPARATORS

The Comparators compare the programmer DO and DI buses. When the DI and DO buses do not compare, a Bit-To-Program signal is output to the control gates. This signal is fed to the Mode Controller ROM, enabling Program operation.

5.2.7 SEQUENCE GENERATOR

The Sequence Generator includes a 4-bit (sequence) counter and a Sequence ROM. Addresses for the Sequence ROM are supplied by the Sequence Counter. Sequence Counter operations are initiated by the Master Clock. The backwards Device Test Memory enables the Sequence Counter for loading, and the Mode Controller enables it for counting.

The Sequence ROM outputs signals that control the analog card, thereby producing waveforms as shown on the timing diagram. The Timing Register synchronizes these ROM outputs so that no glitches are presented to the analog card. Three of the Sequence ROM outputs are fed through the Configure ROM and from this ROM to the Timing Register. The configure ROM adapts these three timing signals to the requirements of the part being programmed. One output of the Configure ROM is a VOL/VOH control line to the analog card.

5.2.8 XTAL 1 OSCILLATOR

This oscillator provides the external timing source for the clock input on the processor parts and is asynchronous to the digital card clock. Its rate is set to a minimum of two times that of the fast rate of the digital clock. This rate ensures sufficient delays (TD) as called out on the Timing Diagram.

5.3 ANALOG CARD

Figure 4-3 gives a generalized block diagram of the analog card. This diagram shows signal flow and functional relationships between the blocks, but does not include detailed interconnection information. Refer to the timing diagram (with truth tables) in Section 4 and the schematics at the rear of this manual for details of circuit connection and operation. The following paragraphs discuss the functions contained on the analog card.

5.3.1 ADDRESS BUFFERS

Address Buffers accommodate the eleven incoming address lines from the programmer MEU. The eight low-order address lines are buffered by noninverting gates with tri-state outputs. These outputs are multiplexed with the outputs of the Data Buffers and with the data lines of the device being programmed. The low-order buffers have an enable input to allow them to present addresses to the device. When disabled, it forces their outputs into the high-impedance state.

The three high-order Address Buffers are noninverting gates with uncommitted collector outputs. These outputs have resistor pull-ups to +5 volts, and tie to a separate port on the device being programmed.

5.3.2 DATA BUFFERS

Data Buffers accommodate the eight incoming DI bus lines from the programmer MEU. These buffers are either inverting or noninverting, as selected by the socket adapter via the digital card Configure ROM. For VOL devices, the buffers are selected as noninverters and for VOH devices as inverters. When enabled, the Data Buffers output data to be programmed to the device.

5.3.3 COMPARATOR AND DO BUS DRIVERS

The Comparator compares programmed data against a reference level. During Read, Comparator outputs are transferred to the DO Bus Drivers. This transfer allows the digital card to compare the device output (DO Bus) and the programmer DI Bus. The DO Bus Drivers are selected as inverters or noninverters by the same means used by the Data Buffers.

5.3.4 SIGNAL BUFFERS

These buffers output the specified timing signals — RD, TO, Reset, ALE and XTAL-1—to the device during Program and Verify operations. The buffers are inverting or noninverting gates with uncommitted collector outputs. These outputs have resistor pull-ups to either the device V_{CC} or +5 volts.

5.3.5 V_{DD} GENERATOR

The V_{DD} Generator is a current-limited regulator with three selectable states. The V_{DD} Program state is selected while programming pulses are being applied to the device. The V_{DD} Verify state is selected during Verify and Read operations. When the programmer is in Stop or Backwards Device Test, the generator is held to a zero voltage state. These levels are selected by signals from the digital card and may be adjusted using potentiometers R9 and R10.

5.3.6 PROGRAM GENERATOR

The Program Generator supplies the specified Program voltage to the PROG or V_{DD} pin of the device under program. The generator has three selectable states: active pull-up to the V_{DD} generator, active pull-down to ground, and high-impedance (float) state. These levels are selected by signals from the digital card.

5.3.7 V_{CC} GENERATOR

The V_{CC} Generator is a two-state regulator that supplies the required voltage to the V_{CC} pin of the device. The generator is an adjustable shunt regulator with an emitter follower. During programmer Stop and Backwards Device Test conditions, its output is held to zero volts. During Program and Read its output is set to the specified value. This value is adjustable using potentiometer R34.

5.3.8 V_{EA} GENERATOR

The V_{EA} Generator is a two-state regulator that supplies the specified V_{EA} voltage to the device. During Stop and Backwards Device Test conditions, the generator output is held to zero volts. During Program and Read, its output is set to the specified V_{EA} voltage. The generator is an adjustable shunt regulator controlled by potentiometer R35.

5.3.9 PROGRAM/CE BUFFER

The buffer outputs the specified Program/CE signal to the part during Verify and Program. The buffer is an inverting gate with an uncommitted collector output and a resistor pull-up to +5 volts.

The timing enable signal for this buffer is the same as for the V_{DD} generator.

5.3.10 CURRENT LIMIT AND RESET CIRCUITS

The V_{DD}, V_{CC} and V_{EA} generators have fold-back current limiting. When the current limit of either supply is reached, Reset is pulled and the supply is shut down. Once Reset is pulled, Stop is held and keeps all supplies shut off.

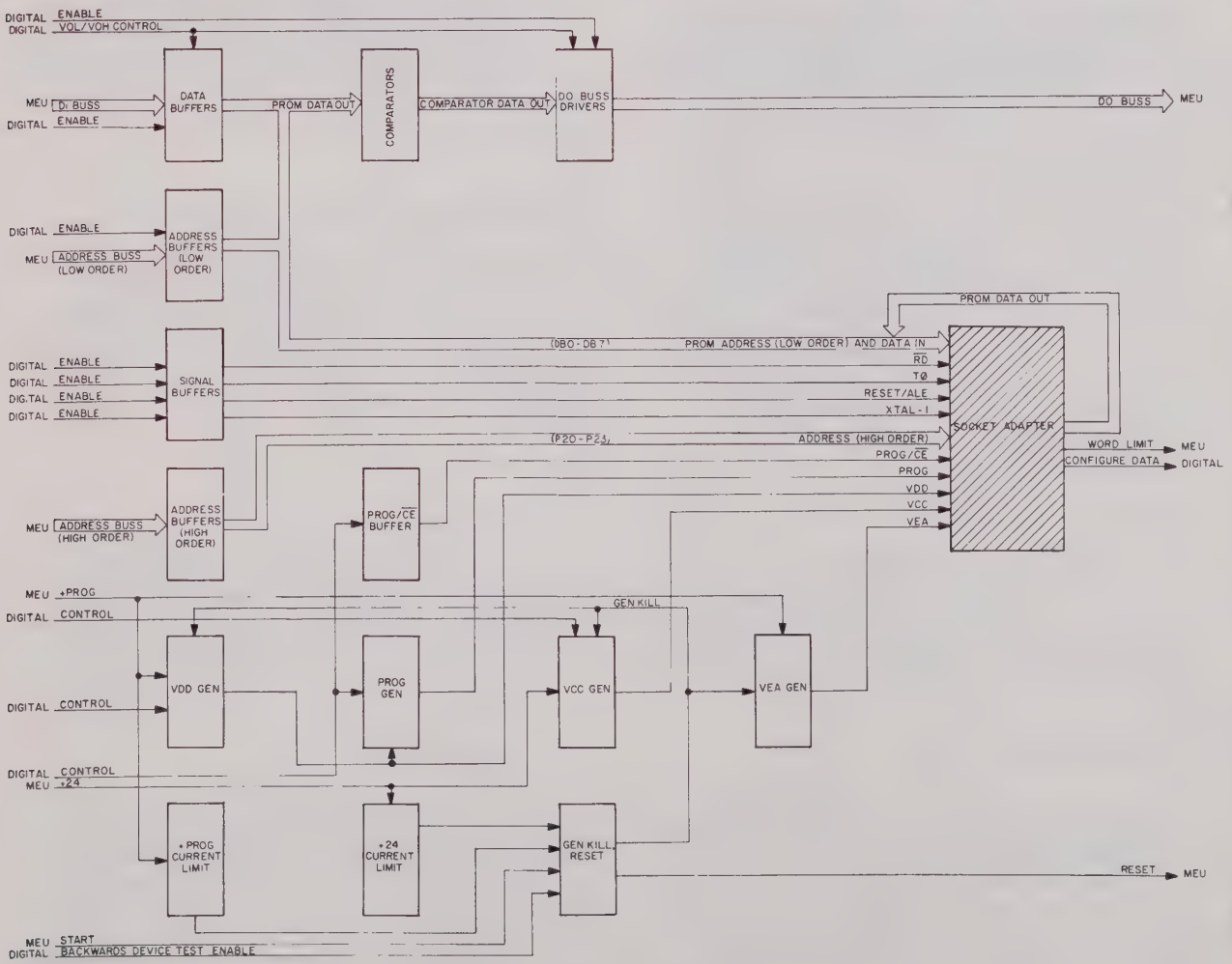


Figure 5-3. Analog Card Block Diagram

SECTION 6
SCHEMATICS

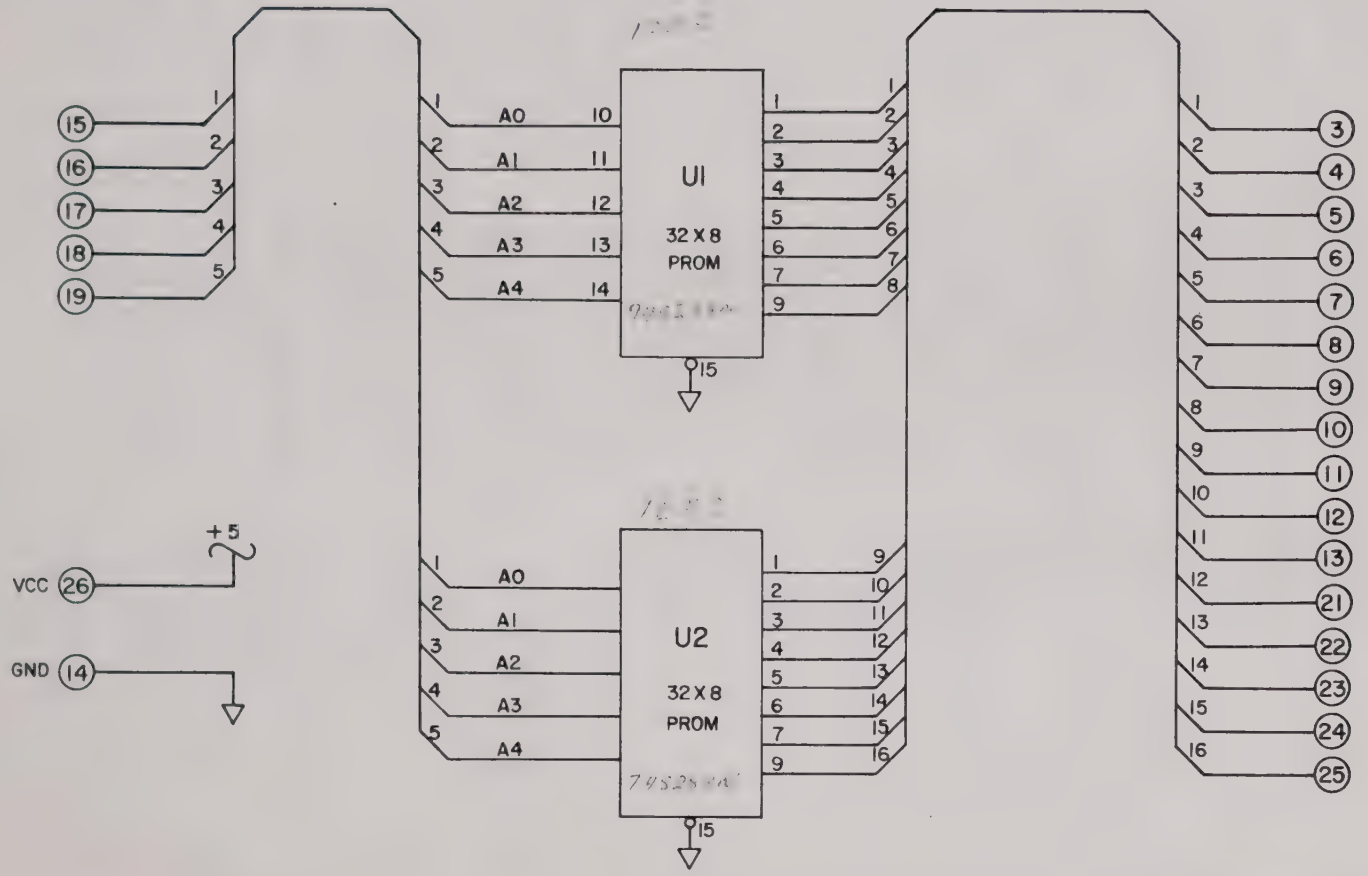
008-1418	Digital Card
008-1417	Analog Card
008-1072	Calibration Adapter

L. ADAPT. EX DATA S. LOGIC) OCATION U 1		TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT			SWITCH POSITIONS		MEASUREMENT				
				DEC	HEX	OCT	S2	S3	TEST PT.	ADJ.	LIMITS MIN	LIMITS NOM	LIMITS MAX
F	DF	ADDRESS TEST VIH, A5	14-18	2730	AAA	5252	7	15	TP3		5.0		5.2
F	DF	ADDRESS TEST VIL, A6	14-19	2730	AAA	5252	7	14	TP3		0.0		0.2
F	DF	ADDRESS TEST VIH, A7	14-20	2730	AAA	5252	7	13	TP3		5.0		5.2
F	DF	ADDRESS TEST VIL, A8	14-21	2730	AAA	5252	7	2	TP3		0.0		0.2
F	DF	ADDRESS TEST VIH, A9	14-22	2730	AAA	5252	7	3	TP3		5.0		5.2
F	DF	ADDRESS TEST VIL, A10	14-23	2730	AAA	5252	7	4	TP3		0.0		0.2
F	DF	ADDRESS TEST VIH, A11	14-24	2730	AAA	5252	7	11	TP3		3.0		5.2
F	DF	VSS TEST	15-1	2730	AAA	5252	8	24	TP3		0.00		0.08
F	FE	VEA LIMIT	16-1	001	01	001	3	23	TP3		7.0		10.0
FF	DF			010	0A	012							
FF	DF			021	15	025							
FF	FF	← DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1417

PAGE 4 OF 4

DATE	SYM	REVISION RECORD	DR	CK
11-13-75	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
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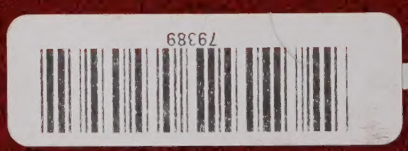

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